What is claimed is:

1. An integrated circuit, comprising:

a multiplicity of macro-circuits, each macro circuit having the same function;

a fuse bank containing a multiplicity of fuses, the state of said fuses storing test data indicating at least which macro-circuits failed a test; and

means for preventing utilization of failing macro-circuits during operation of said integrated circuit.

2. The integrated circuit of claim 1, further including means for isolating inputs and outputs of said macro-circuit during testing of said macro-circuits and during testing of additional circuits of said integrated circuit.

3. The integrated circuit of claim 1, further including isolation circuits adapted to, during testing of said macro-circuits, isolate each macro-circuit from additional circuits of said integrated circuit and couple a single macro-circuit into a single scan chain, the output of said single scan chain observable at an I/O pad of said integrated circuit.

4. The integrated circuit of claim 1, wherein said macro-circuits include logic built-in test circuits.

5. The integrated circuit of claim 1, wherein said means for preventing includes a shift register for reading out the state of said fuses for passing the state of said fuses to a control circuit, said control circuit adapted to disable failing macro-circuits directly or adapted to disable failing macro-circuits under the direction of an electronic system said integrated circuit is electrically connected to.

6. The integrated circuit of claim 5, further including:

one or more repairable circuits, said fuse bank further including additional fuses for storing repair data for said repairable circuits; and

an additional shift register serially connected to said shift register, said additional shift register for reading out the state of said additional fuses and for passing the state of said fuses to a repair circuit, said repair circuit adapted to replace failing portions of said repairable circuits with redundant good circuits.

7. The integrated circuit of claim 1, wherein said macro-circuits are microprocessors and said means for preventing generates a busy signal for each macro-circuit that failed said test.

8. The integrated circuit of claim 1, wherein said fuse bank stores compressed data and further including means for decompressing said compressed data.

9. The integrated circuit of claim 1, wherein said fuses are selected from the group consisting of laser blow fuses, electrical blow fuses or electrical blow antifuses.

10. A method of generating a partial good integrated circuit, the method comprising:

providing an integrated circuit having a multiplicity of macro-circuits arranged in one or more groups, each macro circuit of the same group having the same function, and a fuse bank containing fuses;

isolating said macro-circuits from other circuits of said integrated circuit;

testing each macro-circuit prior to a fuse programming operation;

programming said fuses in said fuse bank in order to store data indicating at least which macro-circuits failed said testing step; and

preventing utilization of each failing macro-circuit during operation of said integrated circuit based on the data stored in said fuse bank.

11. The method of claim 10, wherein:

said integrated circuit further includes first scan chains coupling said other circuits, second scan chains coupled to said macro-circuits and isolation circuits coupled to third scan chains, said isolation circuits coupled between said other circuits and said macro-circuits; and

further including the steps of coupling said first, second and third scan chains into a first configuration to achieve isolation of said other circuits from said macro-circuits and coupling said first, second and third scan chains into a second configuration to achieve isolation of said macro-circuits from each other and from said other circuits.

12. The method of claim 10, wherein said testing includes applying sequentially one or more test patterns to each macro-circuit in each group macro-circuits and determining failing macro-circuits one group at a time.

13. The method of claim 10, further including keeping a count of failing macro-circuits during testing and terminating testing when the number of failing macro-circuits exceeds a predetermined number.

14. The method of claim 10, further including:

writing data indicating at least which macro-circuits failed to a fuse blow file in a tester performing said testing; and

wherein said programming is performed based on data in said fuse blow file.

15. The method of claim 10, further including:

performing a post fuse blow test, said post fuse blow test including in the order recited:

masking each failing macro-circuit based on the data in said fuse bank;

applying sequentially one or more test patterns to each macro-circuit in each group of macro-circuits and determining failing macro-circuits one group at a time; and

terminating post fuse blow test upon any macro-circuit failing.

16. The method of claim 15, further including in the order recited:

after performing said post fuse test, packaging said integrated circuit into a module; and

performing a module test, said module test including in the order recited:

masking each failing macro-circuit based on the data in said fuse bank;

applying sequentially one or more test patterns to each macro-circuit in each group of macro-circuits and determining failing macro-circuits one group at a time; and

terminating module test upon any macro-circuit failing.

17. The method of claim 10, wherein said macro-circuits are microprocessors.

18. The method of claim 10, wherein the step of preventing includes generating a busy signal for each macro-circuit that failed said test.

19. The method of claim 10, wherein the step of preventing includes disabling failing macro-circuits under the direction of an electronic system said integrated circuit is electrically connected to.

20. The method of claim 10, wherein said fuses are selected from the group consisting of laser blow fuses, electrical blow fuses or electrical blow antifuses.